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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/657,141	09/09/2003	Masao Murade	116802	1897

25944 7590 08/25/2005

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EXAMINER	
LANDAU, MATTHEW C	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 08/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/657,141	MURADE, MASAO	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-19* is/are pending in the application.

4a) Of the above claim(s) *14-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-11,13 and 19* is/are rejected.

7)☒ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

This application contains claims 14-18 drawn to an invention nonelected with traverse in the reply filed 1/14/2005. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the capacitor electrode wiring lines must be shown or the feature(s) canceled from the claim(s). No new matter should be entered. Note that the drawings show only one capacitor electrode wiring line.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will

be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 1, 3, 5, 6, 9, and 12 are objected to because of the following informalities:

Regarding claims 1, 6, and 12, the limitation "formed according to intersections" is objected to. It is suggested the limitation be changed to read, "formed at ~~according to~~ intersections", since it is not entirely clear what is meant by having something formed "according to" an intersection.

Regarding claims 3, 5, and 9, a claim cannot depend from a cancelled claim. It is suggested the claims be changed to depend from claim 1.

Further regarding claim 12, the limitation "portions to be the first electrodes of the conductive layers" is objected to. It is suggested this limitation be changed to read, "portions of the conductive layers to be the first electrodes ~~of the conductive layers~~", or "portions to be the first electrodes of the capacitors ~~conductive layers~~", depending on Applicant's intent.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-6, 8-10, 13, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishii (US Pat. 6,404,414).

Regarding claims 1 and 6, Figures 1-4(D) of Ishii disclose an electro-optical device, comprising: data lines 30 extending in a predetermined direction; scanning lines 20 extending orthogonal to the data line; pixel electrodes 55 and pixel switching elements 50 formed according to intersections of the scanning lines and data lines; capacitor electrode wiring lines 84 extending in a direction crossing the data lines; and capacitors 85 including, as first electrodes, conductive layers 87A (Figures 4(B) and 4(D)) connected to the data lines, the capacitors including second electrodes 86 (Figures 4(B) and 4(D)) that include other conductive layers connected to the capacitor electrode wiring lines. Note that the portions of the wiring lines that extend above the transistor shown in Figure 1 (above line 83) can be considered to be part of the data lines. Therefore, the first electrode of the capacitor 85 is connected to the data line without a switching element between the conductive layers and the data lines. Regarding claim 6, Figure 1 of Ishii discloses a data line driving circuit 60 that drives the data lines 30 at one end of the data lines, the capacitors 85 being provided at the other end of the data lines.

Regarding claim 3, the limitation "the capacitor electrode wiring lines having a fixed potential" is merely a functional/intended use limitation that does not structurally distinguish the claimed invention over the prior art. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA

1963). The capacitor electrode wiring lines 84 of Ishii are capable of having a fixed potential if the appropriate voltage is applied.

Regarding claim 4, Figures 1-4(D) of Ishii disclose a substrate 10; a counter substrate (col. 7, lines 59-61) facing the substrate; a counter electrode formed on the counter substrate (col. 7, lines 59-61) and arranged to face the pixel electrodes; and a driving circuit 60/70 arranged on the substrate 10 that drives the scanning lines, the data lines, and the pixel electrodes. It is inherent that a power source (first power source) supplies a potential to the counter electrode and that another power source (second power source) supplies a potential to the driving circuit. Ishii discloses the capacitor electrode wiring lines 84 are connected to the same power source as the counter electrode (the first power source) (col. 7, lines 59-61). The limitations "that supply a fixed potential..." are merely functional/intended use limitations that do not structurally distinguish the claimed invention over the prior. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963).

Regarding claim 5, Ishii discloses the capacitor electrode wiring lines 84 are made of a low resistance material (doped poly) (col. 12, lines 41-44).

Further regarding claim 6, as an alternate interpretation, it can be considered that the transistor shown in Figure 1 (between the top capacitor line 29 and line 83) is the capacitor, since a capacitance inherently exists between the source/drain region and the gate. Therefore, it can be

considered that the first electrode of the capacitor is the source/drain region connected to the data line 30. Using this interpretation, there is no switching element between the conductive layers of the first electrodes and the data lines.

Regarding claim 8, Figures 1-4(D) of Ishii disclose storage capacitors (not labeled) connected to the pixel electrodes and the pixel switching elements. The product-by-process limitation "such that, during manufacturing, at least some of the members forming the capacitors can be formed..." does not structurally/patentably distinguish the claimed invention over the prior art.

Regarding claim 9, the product-by-process limitation "such that, during manufacturing, the capacitor electrode wiring lines and the data lines can be formed in same step", does not structurally/patentably distinguish the claimed invention over the prior art.

Regarding claim 10, Figures 1-4(D) of Ishii disclose bypass layers 81 connected to the data lines 30 and the conductive layers 87A. Ishii further disclose that bypass layers 81 are formed in the same step as the scanning lines 20 (col. 11, lines 17-20).

Regarding claim 13, it can be considered that the data lines 30 (shown in Figure 1 of Ishii) are divided into a plurality of groups, wherein each group comprises two data lines. The limitation "to which image signals are simultaneously supplied" is merely a functional/intended use limitation that does not structurally distinguish the claimed invention over the prior. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use,

then it meets the claim. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963).

Regarding claim 19, it is inherent that the electro-optical device disclose by Figures 1-4(D) of Ishii is part of an electronic apparatus.

Claims 1, 3, 5, 8, 9, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishii. The following rejections are based on an alternate interpretation of Ishii.

Regarding claims 1 and 6, Figures 1-4(D) of Ishii disclose an electro-optical device, comprising: data lines 30 extending in a predetermined direction; scanning lines 20 extending orthogonal to the data line; pixel electrodes 55 and pixel switching elements 50 formed according to intersections of the scanning lines and data lines; capacitor electrode wiring lines 29 extending in a direction crossing the data lines; and capacitors (intersections between data lines 30 and capacitor wiring lines 29) including, as first electrodes, conductive layers (part of data line) connected to the data lines without any switching element between the conductive layers and the data lines, the capacitors including second electrodes (part of capacitor lines 29) that include other conductive layers connected to the capacitor electrode wiring lines. Note that a capacitance inherently exists between the data lines 30 and the capacitor electrode wiring lines 29 at the intersection between these lines. Therefore, it can be considered that the intersections are capacitors, wherein the portions of the lines where the overlap occurs are the respective capacitor electrodes. Regarding claim 6, Figure 1 of Ishii discloses a data line driving circuit 60 that drives the data lines 30 at one end of the data lines, the capacitors (at least some) being provided at the other end of the data lines.

Regarding claim 3, the limitation "the capacitor electrode wiring lines having a fixed potential" is merely a functional/intended use limitation that does not structurally distinguish the claimed invention over the prior art. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963). The capacitor electrode wiring lines 29 of Ishii are capable of having a fixed potential if the appropriate voltage is applied.

Regarding claim 5, it is inherent that the capacitor electrode wiring lines 29 are made of a low resistance material in order to perform their intended function.

Regarding claim 8, Figures 1-4(D) of Ishii disclose storage capacitors (not labeled) connected to the pixel electrodes and the pixel switching elements. The product-by-process limitation "such that, during manufacturing, at least some of the members forming the capacitors can be formed..." does not structurally/patentably distinguish the claimed invention over the prior art.

Regarding claim 9, the product-by-process limitation "such that, during manufacturing, the capacitor electrode wiring lines and the data lines can be formed in same step", does not structurally/patentably distinguish the claimed invention over the prior art.

Regarding claim 19, it is inherent that the electro-optical device disclose by Figures 1-4(D) of Ishii is part of an electronic apparatus.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishii in view of Murade (US PG Pub 2001/0022572).

Regarding claims 7 and 11, Figure 1 of Ishii discloses a data line driving circuit 60 that drives the data lines at one end of the data lines. The difference between Ishii and the claimed invention is a test circuit that checks the operation of the electro-optical device at the other end of the data lines. Murade discloses a test circuit in the peripheral area of an electro-optic device (page 18, paragraph [0165]). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Ishii by including test circuit for the purpose of testing the quality or detect a defect in the liquid crystal apparatus during the production process or before shipment (page 18, paragraph [0165] of Murade).

Allowable Subject Matter

Claim 12 would be allowable if rewritten to overcome the claim objections set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record, either singularly or in combination, does not disclose or suggest the combination of limitations including capacitors including, as first electrodes, conductive layers connected to the data lines without any switching element between the conductive layers and the data lines; and portions to be the first electrodes of the conductive layers being wider than the data lines.

Response to Arguments

Applicant's arguments filed 6/10/2005 have been fully considered but they are not persuasive.

The above rejections are essentially new grounds of rejection since they are based on new interpretations of the Ishii reference. In response to Applicant's argument that Ishii does not disclose "capacitors including, as first electrodes, conductive layers connected to the data lines without any switching element between the conductive layers and the data lines", as explained in the above rejection, Ishii does disclose this claimed feature. Under one interpretation, it is considered that the data line includes the wiring between the transistor shown in Figure 1 of Ishii and the capacitor 85. Therefore, the first electrodes are connected to the data lines without a switching element in between. Under another interpretation, it is considered that the capacitors are formed at the intersection of the capacitor lines 29 and the data lines 30, since the intersection between the wiring lines inherently has a capacitance. Therefore, the first electrode, which is part of the data line, is connected to the data line without a switching element in between.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew C. Landau

August 20, 2005

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER